REMARKS/ARGUMENTS

In reviewing the application as filed, certain inadvertent errors were noted which have been corrected herein. First, Figure 6 identifies block B2 as an "N-type Current mode Current Sensing" block, whereas page 10 referred to Figure 4 for Block B2. It may be seen that Figure 4 is a P-type Current mode Current Sensing circuit, whereas Figure is the N-type Current mode Current Sensing" block. Appropriate correction of the Figure reference has now been made.

Also starting on line 13, page 12, when discussing Figure 10, a condition is set forth under which the current through transistor MP3 supposedly will be equal to I3. Looking at Figure 10, it is apparent that the current through transistor MP3 will always be I1. Accordingly the associated portion of the relevant paragraph on page 12 has been amended. In that regard, no new matter has been added, as the revision is simply a statement of what a simple circuit analysis shows.

In response to the rejections of certain claims under 35 USC Sec 112, claim 1 has been amended to eliminate the double recitation of the same limitation. Claim 5 has been amended to set forth that the biasing circuitry referred to is part of the second control loop.

With respect to claim 6, the examiner states it is unclear whether the voltage of the second power supply and the reference voltage are the same or different. If the two voltages were identical, they would have been given the same identification. In the circuit embodiments shown, the reference voltage is the voltage across R1. As to the third control loop, reference is made to the embodiment of Figure 5, not Figure 2. In that Figure, the first control loop is comprised of transistors MP1, MP3, MP5, MP6 and the buffer amplifier. The second loop is comprised of transistors MP3, MP4 and MP7, and the third loop is comprised of transistors MP11, MP12, MN1, MN2 and MN8. In that regard, the examiner's attention is directed to the description of Figure 5, starting on line 11 of page 9 of the application.

Claim 7 has been carefully amended to claim the combination of blocks B1 and B2 of Figure 6. Claim 9 has been amended to add the current mirror (Block B3 of Figure 6) and the output resistor R.

Claims 14 through 18 are cancelled.

Finally, the Examiner rejected claim 20 under 35 USC § 112, though it is believed that the Examiner intended to refer to claim 19, not 20. Claim 19 has been amended herein in accordance with the Examiner's comments.

CONCLUSION

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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